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USING CLOCK AND DATA RECOVERY PHASE ADJUST TO SET LOOP DELAY OF A DECISION FEEDBACK EQUALIZER

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/530,968, entitled "USING CLOCK AND DATA RECOVERY PHASE ADJUST TO SET LOOP DELAY OF A DECISION FEEDBACK EQUALIZER", filed December 19, 2003, the disclosure of which is incorporated herein by reference.

This application is related to U.S. Provisional Patent Application Serial No. 60/531,403, entitled "CONTINUOUS TIME FILTER-DECISION FEEDBACK EQUALIZER ARCHITECTURE FOR OPTICAL CHANNEL EQUALIZATION", filed December 19, 2003; and U.S. Provisional Patent Application Serial No. 60/531,402, entitled "DECISION FEEDBACK EQUALIZER AND CLOCK AND DATA RECOVERY CIRCUIT FOR HIGH SPEED APPLICATIONS", filed December 19, 2003, the disclosure of each of which is incorporated herein by reference.

BACKGROUND

Many high speed serial communication systems only transmit data over a communication media. In other words, these systems do not transmit clocks signals that may be used by a receiver to recover the data. Consequently, receivers for high speed serial communication systems often include a clock and data recovery circuit that produces a clock signal synchronized with the incoming data. The clock is then used to sample or recover the individual data bits.

In operation however, bandwidth limitations inherent in many communication media tend to create increasing levels of data distortion with increasing data rate and channel length. For example, band-limited channels tend to spread transmitted pulses. If the width of the spread pulse exceeds a symbol

duration, overlap with neighboring pulses may occur, degrading the performance of the receiver. Therefore, typical high speed receivers may also include an adaptive equalizer, such as, for example, a decision feedback equalizer that removes or reduces channel induced inter-symbol interference.

In conventional receivers the extracted clock from the clock and data recovery circuit drives a retimer of the decision feedback equalizer to recover equalized data. However, variations in the delay along the processing path of the decision feedback equalizer can cause the clock and data recovery circuit to lose synchronization with the incoming data.

SUMMARY

In one aspect of the present invention a communication system includes a decision feedback equalizer adapted to reduce channel related distortion in received data and a clock and data recovery circuit coupled to the equalizer which generates an extracted clock signal having an adjustable phase offset from the equalized data to compensate for processing delays in the equalizer. In this aspect of the present invention the decision feedback equalizer includes a retimer that generates recovered equalized data from the equalized data in response to the extracted clock signal.

In another aspect of the present invention a communications system includes a decision feedback equalizer adapted to reduce channel related distortion in received data, a clock and data recovery circuit and a real time optimizer. In this aspect of the present invention a clock and data recovery circuit coupled to the equalizer generates an extracted clock signal from the equalized data. A retimer of the decision feedback equalizer then generates recovered equalized data from the equalized data in response to the

extracted clock signal. In this aspect of the present invention the communications system further includes a real time optimizer coupled to the clock and data recovery circuit that generates a phase adjust signal, wherein the clock and data recovery circuit adjusts phase of the extracted clock signal in response to the phase adjust signal to compensate for processing delays in the decision feedback equalizer.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will become better understood with regard to the following description, appended claims, and accompanying drawings, in which:

FIG. 1 is a simplified block diagram of a high speed receiver having an integrated decision feedback equalizer and a clock and data recovery circuit in accordance with an exemplary embodiment of the present invention;

FIG. 2 is an open loop diagram of the receiver of FIG. 1 in accordance with an exemplary embodiment of the present invention;

FIG. 3 is a timing diagram at a plurality of points along the open loop diagram of FIG. 2 graphically illustrating one example of processing delay through the receiver elements in accordance with an exemplary embodiment of the present invention;

FIG. 4 is a simplified block diagram of a clock and data recovery circuit with an adjustable phase offset for use in the receiver of FIG. 1 in accordance with an exemplary embodiment of the present invention;

FIG. 5 is a simplified block diagram of high speed receiver having an integrated decision feedback equalizer and a clock and data recovery circuit and an error generation circuit for optimizing adjustable phase offset of the clock

and data recovery circuit in accordance with an exemplary embodiment of the present invention;

FIG. 6 is a simplified block diagram of a clock and data recovery circuit with an adjustable delay for use in the receiver of FIG. 1 in accordance with an exemplary embodiment of the present invention; and

FIG. 7 is a simplified block diagram of an optical communication system in accordance with an exemplary embodiment of the present invention.

In accordance with common practice the various features illustrated in the drawings are not to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. In addition like reference numerals denote like features throughout the specification and figures.

DETAILED DESCRIPTION

Some embodiments of the present invention provide a high speed receiver with clock and data recovery and decision feedback equalization. Referring to FIG. 1, in one embodiment a one tap decision feedback equalizer 110 is combined with a clock and data recovery circuit 120 to provide a high performance receiver 100. In this embodiment summer 130 combines an incoming data signal 140 with an equalized feedback signal 150. A slicer 160 converts the output of the summer (soft decision) to a binary signal 160(a).

In this embodiment, the binary signal output by the slicer 160 directly drives the data input of flip flop 170 as well as a clock and data recovery circuit 120. The clock and data recovery circuit 120 therefore generates an extracted clock signal from the binary signal 160(a) output by the slicer rather than from the incoming data 140 as is done in conventional receivers. The extracted clock output by the

clock and data recovery circuit 120 is then used to clock the decision feedback equalizer flip flop 170 that recovers the data from the binary signal 160(a) in response to the extracted clock.

Therefore, the clock and data recovery circuit 120 automatically aligns the rising edge of the extracted clock, for example, with transitions in the binary signal 160(a) output by the slicer 160. Therefore, the illustrated embodiment maintains the proper timing relationship between the flip flop 170 drive data and clock (i.e. the extracted clock) to ensure proper data recovery without the need for additional delay matching stages.

In the illustrated embodiment a multiplier 180 again scales the recovered equalized data output by the flip flop 170 by an equalization coefficient (g1) to generate the equalized feedback signal 150. The value of the equalization coefficient depends on the level of inter-symbol interference that is present in the incoming data. Typically the absolute value of the equalization coefficient (usually a negative number) increases with increasing inter-symbol interference. In one embodiment a real time optimization loop (not shown), such as a least mean square optimization loop monitors the bit error rate of the incoming signal and adjusts the value of the equalization coefficient in response to changes in the bit error rate.

Summer 130 then combines the equalized feedback signal 150 (typically a negative number) with the incoming data 140. The summer therefore subtracts a scaled version of the previous symbol from a current symbol to reduce or eliminate channel induced distortion such as inter-symbol interference. Therefore, in this embodiment, equalized data (i.e. data that has been processed to remove inter-symbol interference) drives the clock and data recovery circuit 120.

As a result, the clock and data recovery circuit 120 more readily locks onto the binary signal 160(a) as compared to a conventional receiver that locks onto than the incoming data. However, in this embodiment the delay along the processing path of the decision feedback equalizer may cause the clock and data recovery circuit to loose synchronization with the binary signal, thereby corrupting the output of the receiver.

For example, FIG. 2 is an open loop diagram of the decision feedback equalizer of FIG. 1 with the processing path interrupted at the input to the decision feedback flip flop 170 which in this example is timed by clock signal 210 (CLK). FIG. 3 graphically illustrates one example of timing waveforms at various points along the processing path of the open loop diagram of FIG. 2. In operation the various components of the decision feedback equalizer add delay along the processing path of the equalizer.

For example, in this embodiment the decision feedback flip flop 170 latches input data signal (D1) in response to a clock signal (CLK). In the embodiment of FIG. 2 a clock and data recovery circuit 120 may be used to generate a flip flop clock signal (CLK) 210 having its leading edge aligned with the transition edges of the flip flop data signal (D1). However, practical limitations in the design and implementation of the clock and data recovery circuit typically result in a slight offset between the phase of the input data signal (D1) and the clock signal (CLK). In one embodiment the flip flop 170 latches on the falling edge of clock signal (CLK) to generate a flip flop output signal (D2) after a flip flop clock to Q delay (illustrated as t_{C2Q} in the open loop timing diagram of FIG. 3). In this embodiment the phase offset between the transition in the input data signal (D1) and the falling edge of the flip flop clock signal is denoted t_{D2C} in the open loop timing diagram of FIG. 3.

Similarly summer 130 combines a feedback equalization signal with incoming data to generate soft decision (D3) having a summer delay (t_{SU}) with respect to the equalization signal (D2). In this embodiment the summer output (D3) drives a slicer that adds a slicer delay illustrated as (t_{SL}). Therefore the total delay (t_{DFE}) along the processing path of the decision feedback equalizer may be represented as given in Eq. (1) below:

$$t_{DFE} = t_{D2C} + t_{C2Q} + t_{SU} + t_{SL} \qquad (1)$$

Thus, if the total delay along the decision feedback equalizer loop (t_{DFE}) is equal to a full period, the transition edge of the binary signal output by the slicer (D4) is properly aligned with the transition point of previous flip flop input (D1). However, if the total delay along the decision feedback equalizer loop (t_{DFE}) is not equal to a full period then the transition edge of the binary signal output by the slicer (D4) is shifted relative to the transition edge of previous flip flop input (D1).

Moreover, in this instance, the clock and data recovery circuit 120 shifts the leading edge of the extracted clock signal (CLK) 210 to align it with the input data (D4). The shift in leading edge of the extracted clock signal (CLK) in turn alters the separation (t_{D2C}) between the transition in the input data signal (D1) and the falling edge of the flip flop clock signal as well as the total delay (t_{DFE}) along the processing path of the decision feedback equalizer..

In practice, the total shift (ΔCLK) in the extracted clock signal (CLK) is proportionate to the equalization coefficient (g1) if the total delay (t_{DFE}) along the processing path of the decision feedback equalizer is not equal to one period of the incoming data as detailed below in Eq. (2).

$$\Delta CLK = K * (T - t_{DFE})^2 \qquad (2)$$

where K is a constant that is proportional to the equalization coefficient (g1). Thus, if the total delay (t_{DFE}) along the processing path of the decision feedback equalizer is not equal to one period of the incoming data then the shift in the extracted clock signal increases with increasing levels of equalization (i.e. as g1 and therefore K increase). In operation, if the shift in the extracted clock becomes too large the clock and data recovery circuit may lose synchronization with the incoming data and the receiver possibly corrupting the output of the receiver.

In addition, the shift between the delay along the processing path of the decision feedback equalizer and the period (T) of the incoming data that maximizes receiver performance may not be zero but rather may be dependent upon the received data. Therefore, a high speed receiver in accordance with an exemplary embodiment of the present invention adjusts the total delay along the processing path of the decision feedback equalizer to provide higher receiver performance.

For example, in one embodiment a clock and data recovery circuit generates an extracted clock that has the same frequency as an incoming data signal. The clock and data recovery circuit further aligns one of the edges of the extracted clock, such as for example, the rising edge, with the transition edge of the incoming data signal. In this embodiment the clock and data recovery circuit also adjusts the phase of the extracted clock signal to optimize the total delay along the processing path of the decision feedback equalizer to reduce the receiver bit error rate and sensitivity to inter-symbol interference.

FIG. 4 is a simplified block diagram of a clock and data

recovery circuit 400 for generating an extracted clock signal 405 having a frequency that is synchronized with the frequency of the incoming data 410 and having a variable phase. In this embodiment the clock and data recovery circuit 400 includes a phase detector 420 that receives, by way of example, the incoming data signal 410 (e.g. the binary signal 160(a) output by the slicer of FIG. 1) on a first input and the output 405 of a voltage control oscillator 450 at a second input. In one embodiment, the phase detector 420 determines a phase relationship between the output 405 of the voltage control oscillator 450 and the incoming data signal 410.

For example, in one embodiment the phase detector 420 compares transitions in the incoming data signal 410 to the rising edges or the falling edges of the output 405 of the voltage control oscillator 450. The phase detector 420 then produces, by way of example, a phase error signal that is proportional to the phase relationship between the two input signals.

A charge pump 430 then generates a current signal having a magnitude that varies as a function of the magnitude of the error signal generated by the phase detector 420. A loop filter 440 then filters out the high frequency components of the current signal output by charge pump 430 and forwards the filtered signal to the voltage controlled oscillator 450.

In one embodiment, if the incoming data signal 410 leads the output signal 405 of the voltage control oscillator 450, the frequency of the output signal 405 of the voltage controller oscillator 450 is less than the frequency of the incoming data signal 410. In this instance, the charge pump 430 increases its output current to provide a control signal which increases the frequency of the output signal 405 of the voltage control oscillator 450.

As the frequency of the output signal 405 of the voltage

control oscillator 450 increases, its edges come sooner in time (i.e., the edges advance in time). Thus, for example, the rising edges of the output signal 405 of the voltage control oscillator 450 come in better alignment with the transitions or other reference points in the incoming data signal 410. Thus, the feedback may insure that the incoming data signal and the output signal of the voltage control oscillator have the desired frequency relationship for retiming the incoming data via a data retimer (e.g. flip flop 170 of FIG. 1).

In addition, in one embodiment a phase adjust signal 460 may be used to create an offset in the detected phase relationship between the incoming data signal and the output of the voltage control oscillator. For example, if the phase of the incoming data signal 410 and the output signal 405 of the voltage control oscillator 450 were perfectly aligned and the offset injection signal called for a five degree phase offset, the phase detector 420 would output a phase error signal corresponding to a five degree phase difference between the two signals.

Channel induced distortions may also increase the receiver's bit error rate. As a result, signal distortion may be such that in some embodiments the optimum value of the total delay along the processing path of the decision feedback equalizer may not be exactly equal to one period of the incoming data. Therefore, in one embodiment, the phase adjust signal may be optimized to compensate for the delay along the processing path of the decision feedback equalizer as well as channel induced distortion in the received signal.

For example, the high speed receiver 500 illustrated in FIG. 5 includes, by way of example a monitor circuit 505 that tracks the distortion in the soft decision data output by the summer 130 of the decision feedback equalizer. In this embodiment the monitor circuit 505 generates a distortion

error signal 505(a) from the soft decision data that may be used by a real time optimizer 550 to adjust the phase offset signal of the clock and data recovery circuit 120 to improve the performance of the receiver 500.

In one embodiment the monitor circuit 505 may include an analog to digital converter 510 that converts the analog soft decision signal output by the summer 130 of the decision feedback equalizer to a digital signal. In one embodiment the analog to digital converter samples the analog soft decision at a relatively low rate in response to a low speed reference clock. The reference clock 520 may be, for example, a low-frequency signal generated by a stable oscillation source (e.g., a crystal).

In one embodiment a delay lock loop (not shown) may be used to align the transition edges of the low frequency reference clock 520 with the transition edges of the clock signal which clocks the flip flop 170 of the decision feedback equalizer to ensure that the monitor circuit 505 is properly synchronized with the decision feedback equalizer. A delay lock loop which is suitable for synchronizing the reference clock 520 and clock 260 is disclosed in commonly owned U.S. Provisional Patent Application Serial No 60/531,095 entitled "HIGH FREQUENCY BINARY PHASE DETECTOR", filed December 19, 2003, the disclosure of which is incorporated herein by reference.

A digital limiter 530 compares the quantized soft decision output by the analog to digital converter 510 with a threshold and generates a binary signal (e.g., one or minus one) having a low value if the quantized signal is less than the threshold and a high value if the quantized signal is greater than or equal to the threshold. A combiner 540 generates an error signal 540(a) by subtracting the quantized soft decision 510(a) output by the analog to digital converter

with the binary signal 530(a) output by the digital limiter.

In some embodiments the error signal 540(a) is squared and then accumulated to generate a sum square error signal. In this embodiment, a real time optimizer 550 may be used to reduce the value of the sum square error signal as a function of the phase offset of the clock and data recovery circuit 120.

One of skill in the art will appreciate that the phase of the clock and data recovery circuit may be adjusted in a variety of ways. For example, FIG. 6 is a simplified block diagram of a clock and data recovery circuit 600 that includes a delay 610 coupled between the voltage control oscillator 450 and the phase detector 420 to adjust the phase of the extracted clock signal output by the oscillator 450 to compensate for changes in the delay along the processing path of the decision feedback equalizer of FIG. 1. In this embodiment a real time optimizer 550 may again be used to vary the delay through delay element 610 to reduce the sum square error of the equalized data as previously described with respect to FIG. 5.

The integrated decision feedback equalizer and clock and data recovery circuit of the present invention may be integrated into any of a variety of applications. For example, referring to FIG. 7, the described exemplary integrated decision feedback equalizer and clock and data recovery circuit may be incorporated into an optical receiver assembly 710 of an optical communication system 700. The optical system 700 includes an optical transmitter 720 and an optical fiber network 730 that carries the optical signal to the optical receiver assembly 710. Those skilled in the art will appreciate that the present invention is not limited to a single optical transmitter and receiver. Rather practical optical communications systems may have one or more optical

transmitters as well as one or more optical receivers.

The illustrated receive path includes an optical detector 735, sensing resistor 740, one or more amplifiers 750, clock and data recovery circuit 760, and decision feedback equalizer 765. The optical detector 735 can be any known prior art optical detector. Such prior art detectors convert incoming optical signals into corresponding electrical output signals that can be electronically monitored.

A transmit path includes, by way of example, one or more gain stage(s) 770 coupled to an optical transmitter 775. In one embodiment an analog data source provides an analog data signal that modulates the output of the optical transmitter In other embodiments baseband digital modulation or frequency modulation may be used. In this embodiment the gain stage(s) amplify the incoming data signal and the amplified data signal in turn drives the optical transmitter 775.

The gain stage 770 may have multiple stages, and may receive one or more control signals for controlling various different parameters of the output of the optical transmitter. The optical transmitter may, for example, be a light emitting diode or a surface emitting laser or an edge emitting laser that operates at high speeds such as 10 Gigabits per second (Gbps) or higher.

A receive fiber optic cable 730 carries an optical data signal to the optical detector 735. In operation, when the transmit optical beam is incident on a light receiving surface area of the optical detector, electron-hole pairs are generated. A bias voltage applied across the device generates a flow of electric current having an intensity proportional to the intensity of the incident light. In one embodiment, this current flows through sensing resistor 740, and generates a voltage.

The sensed voltage is amplified by the one or more

amplifier(s) 750. The output of amplifier 750 drives the decision feedback equalizer 765. As illustrated in FIG, 5, the decision feedback equalizer, includes, by way of example, a slicer that generates a binary signal that drives the clock and data recovery circuit. The clock and data recovery circuit generates an extracted clock signal from the binary signal which is coupled to a decision feedback equalizer retimer (as illustrated in FIG. 5) to retime the equalized data.

It will be appreciated by those of ordinary skill in the art that the invention can be embodied in other specific forms without departing from the spirit or essential character thereof. Thus, the teachings herein may be applied to different receivers, decision feedback equalizers and clock and data recovery circuits. For example, delay may be provided for the clock and data recovery circuits using a variety of delay techniques. The present invention is therefore considered in all respects to be illustrative and not restrictive. The scope of the invention is indicated by the appended claims, and all changes that come within the meaning and range of equivalents thereof are intended to be embraced therein.